Problems Related to Adder

Q) If a half adder is designed using only NAND gates and if a Single NAND gate delay is 2 μsec, what is the minimum possible propagation delay for the H.A ?

① Ans: 6 μsec., 5

What is the minimum number of NAND Gates require to realize?

A B → H.A → Sum → $A \oplus B$

H.A → Carry → AB

NAND → Universal Gate

$A \oplus B = \bar{A}B + A\bar{B}$

$= \overline{(\bar{A}B + A\bar{B})}$

$= \overline{\bar{A}B} \cdot \overline{A\bar{B}}$

$\bar{A} \rightarrow 1$

$\bar{B} \rightarrow 1$

Sum = 5 NAND

Carry = 2 NAND

7 NAND

$= A \oplus B$

NAND → XOR

$= A\bar{B} + \bar{A}B$

$\overline{A \cdot B}$

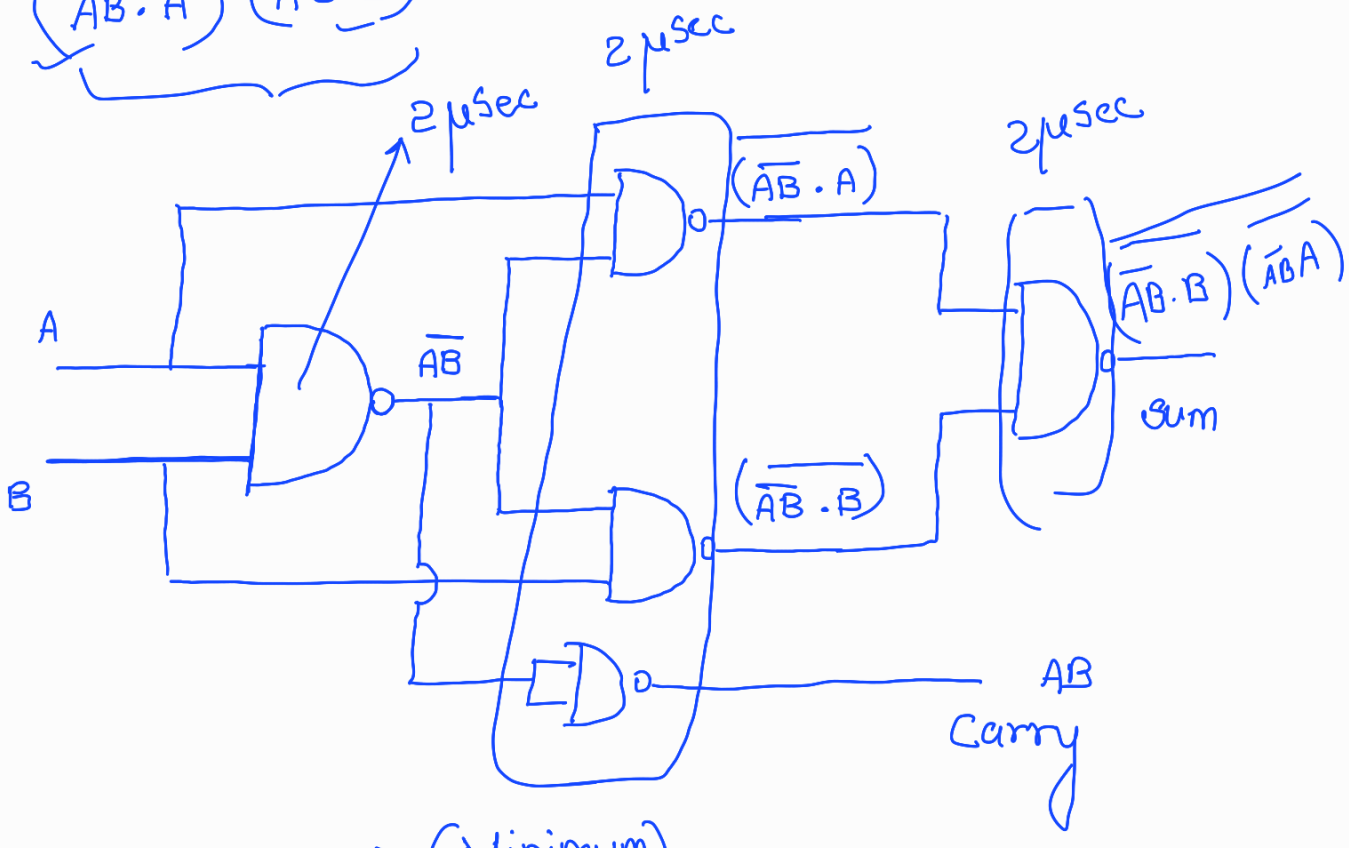
$= (\bar{A}+\bar{B})A + (\bar{A}+\bar{B})B$

$= \cancel{\bar{A} \cdot A}^{\,0} + \bar{B} \cdot A + \bar{A} \cdot B + \cancel{\bar{B} \cdot B}^{\,0}$

$(\bar{A}+\bar{B})A + (\bar{A}+\bar{B})B$

$= \overline{A\bar{B} \cdot A} + \overline{A\bar{B} \cdot B}$

$= \overline{(\overline{A\bar{B} \cdot A})(\overline{A\bar{B} \cdot B})}$



Total 5 NAND (Minimum)

NAND Gate = 2μsec

2 + 2 + 2 = 6μsec.

NOR, Multiplexer, Decoder, etc.

(2) Prove :- $\overline{AB + BC + CA} = AB + C(A \oplus B)$

A
B
C_{in}

For a full adder if inputs are A, B and C_{in}

$$Sum = A \oplus B \oplus C_{in}$$

$$Carry = AB + BC_{in} + C_{in}A$$

$\bar{A} + A = 1$

$1 \cdot A = A$

$A + A = A$

L.H.S :- $AB + BC + CA$

$= AB + \underbrace{(\bar{A} + A)BC}_{BC} + \underbrace{(\bar{B} + B)CA}_{CA}$

$= AB + \bar{A}BC + ABC + \bar{B}CA + BCA$

$= AB + C(\bar{A}B + \bar{B}A) + ABC + BCA$

$= AB + C(A \oplus B) + ABC + BCA$

$= AB[\underbrace{1 + C + C}_{1}] + C(A \oplus B)$

$= AB + C[A \oplus B]$ R.H.S

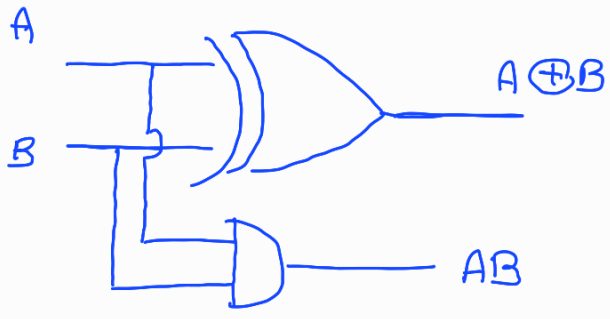
Can you design a full adder using half adders ?

H.A = Sum = $A \oplus B$

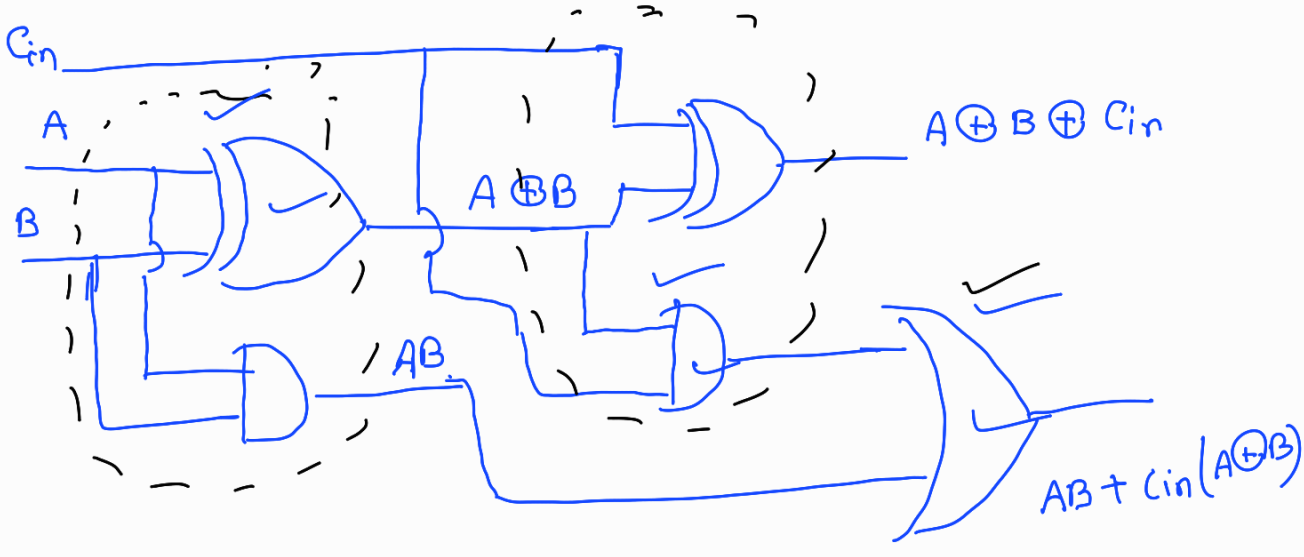
(A, B) Carry = AB

$AB + BC_{in} + C_{in}A$

$= AB + C_{in}(A \oplus B)$



2 H.A.

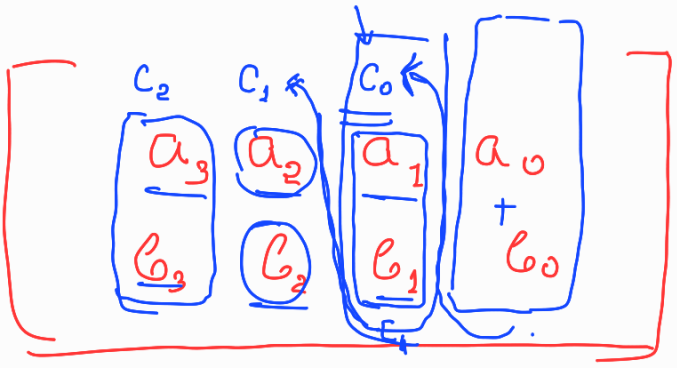


Q) A half adder (H.A) is implemented using XOR and AND Gate. A full adder is implemented using 2 H.A and one OR gate,

$$P_{XOR} = 2\,P_{AND} \longrightarrow (1)$$

$$P_{AND} = P_{OR} = 1.2\ \mu sec$$

What is the propagation delay for a binary CLA adder where inputs are 4 bits numbers.



Solution

delay Sum = 2.4 μsec + 2.4 μsec = 4.8 μsec

delay Carry = 2.4 μsec + 1.2 μsec + 1.2 μsec = 4.8 μsec.

$$P_{XOR} = 2 \times 1.2 = 2.4\ \mu sec.$$

$$3 \times 2.4\ \mu sec. = 7.2\ \mu sec$$

$4.8\,\mu sec + 7.2\,\mu sec = 12\,\mu sec$

Here, Since $a_1, a_2, a_3, b_1, b_2, b_3$ are present before hand So only Second H.A will wait for Carry computation of previous bit. So total $= 3 \times 2.4\,\mu sec$ for rest 3 bits Sum computation.

final propagation delay $= 3 \times 2.4\,\mu sec + 4.8\,\mu sec.$

$= 12\,\mu sec.$