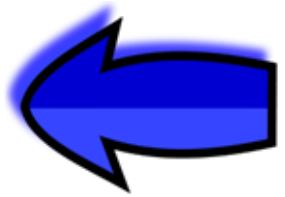
Chapter 7: A Primer On Digital Logic

Basic Computer Architecture

Outline

* Transistors and Gates



* Combinational Logic
* Sequential Logic
* SRAM/ DRAM Cells

Disclaimer: This chapter is only to get a high level overview …

- We assume some background in logic gates, transistors, combinational and sequential logic
- The aim of this chapter is to only provide a high level overview
- For a deeper understanding consult any of the classic textbooks on digital logic

Atoms and Molecules of Circuits

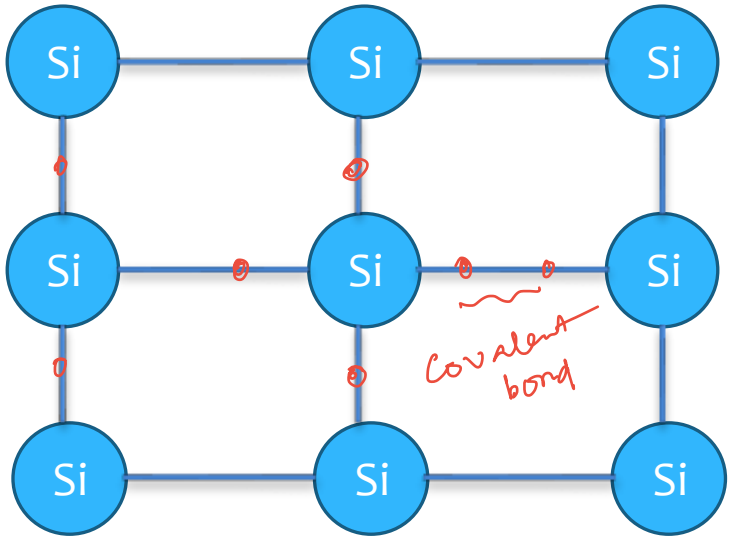
The Transistor

- It is just a **switch**.
- It is either switched on (current can flow), or switched off (no current flow)

How is a Transistor Made?

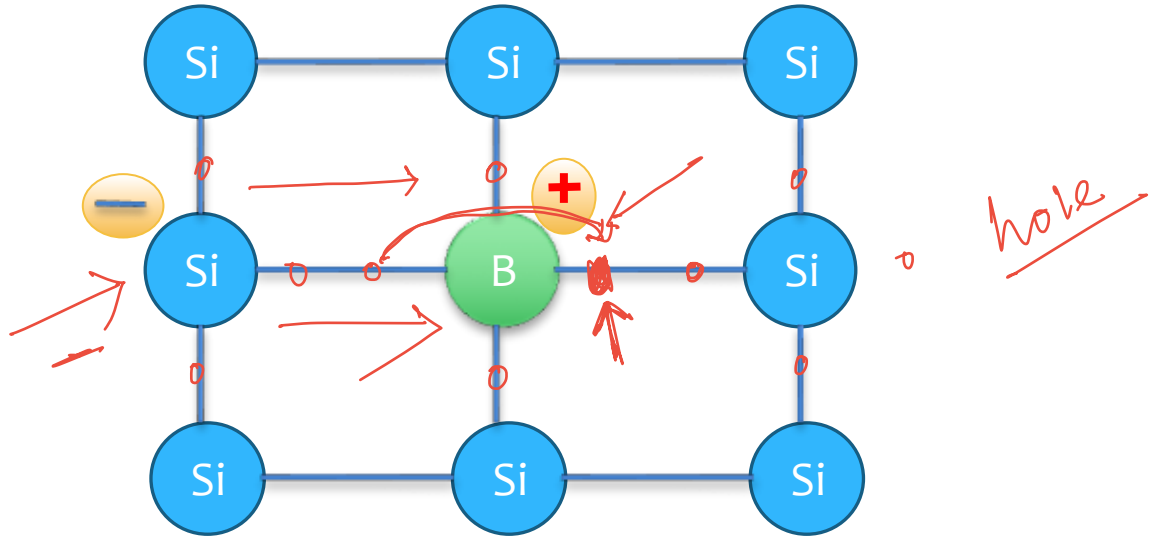
* It is made of Silicon
  * Silicon is a semi-conductor (neither conductor or insulator).
  * We can change its properties:
  * Add a little bit of impurities → doping
* Dope it with Group III elements (3 valence electrons)
  * Boron, Aluminum and Gallium
  * It is called a p-type semiconductor
* Or, dope it with Group V elements (5 valence electrons)
  * Phosphorus or Arsenic
  * It is called a **n-type** semiconductor

Silicon Lattice



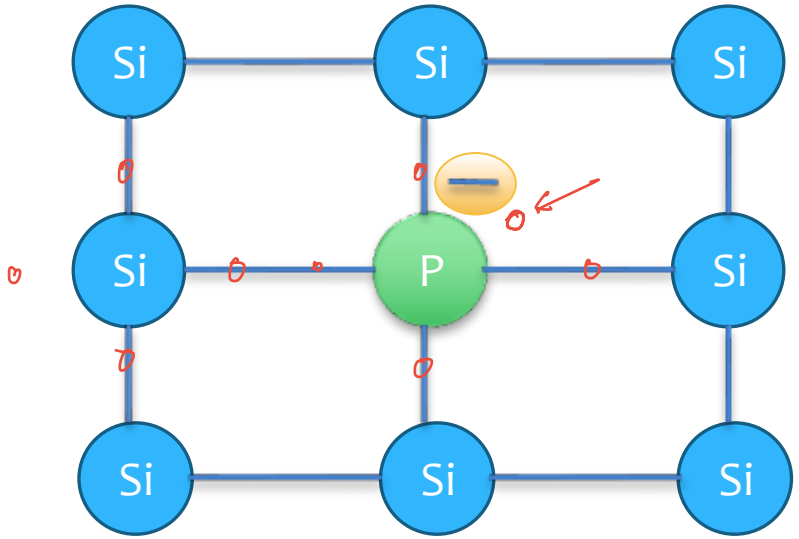
* This is a typical silicon lattice. Each Si atom is connected to 4 other atoms via covalent bond

P-Type Doping



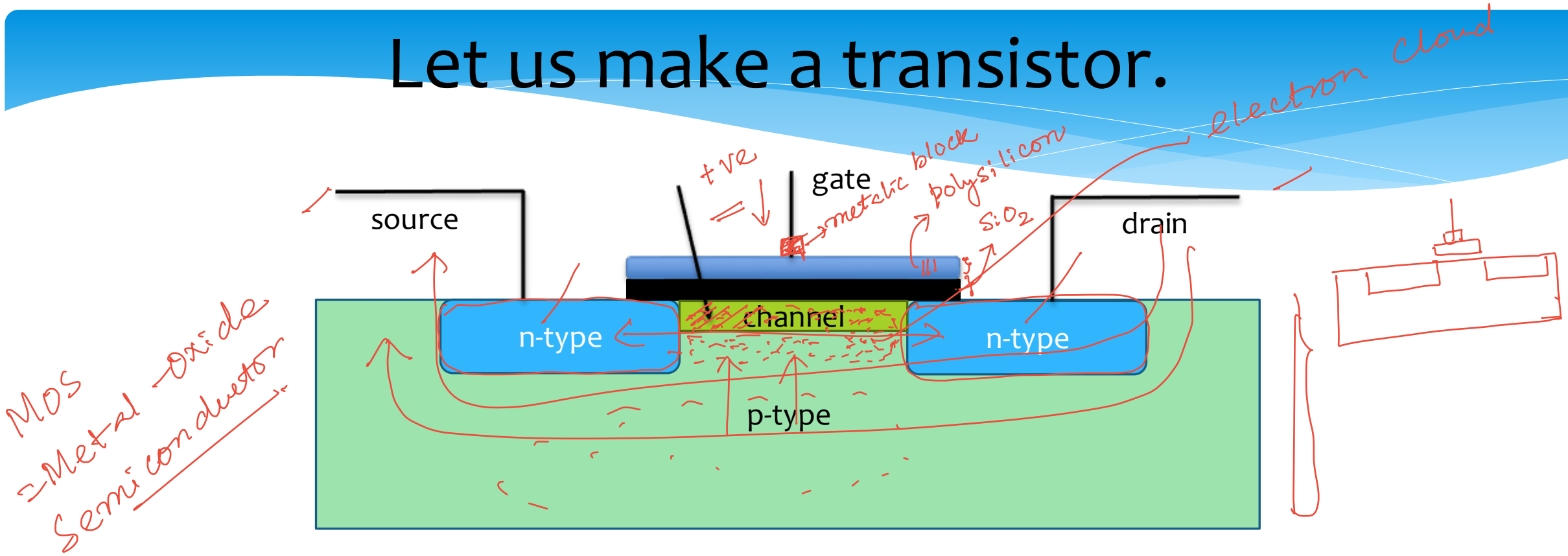
* If there is a Boron atom in the lattice. It will create bonds with the rest of the atoms.
* There will be one less electron (hole)
* Holes can flow. They are associated with +ve charge. (see the animation)

N-Type Doping



* If there is a Phosphorus atom in the lattice. It will create bonds with the rest of the atoms.
* There will be one more electron (electron)
* Electrons can flow. They are associated with -ve charge. (see the animation)

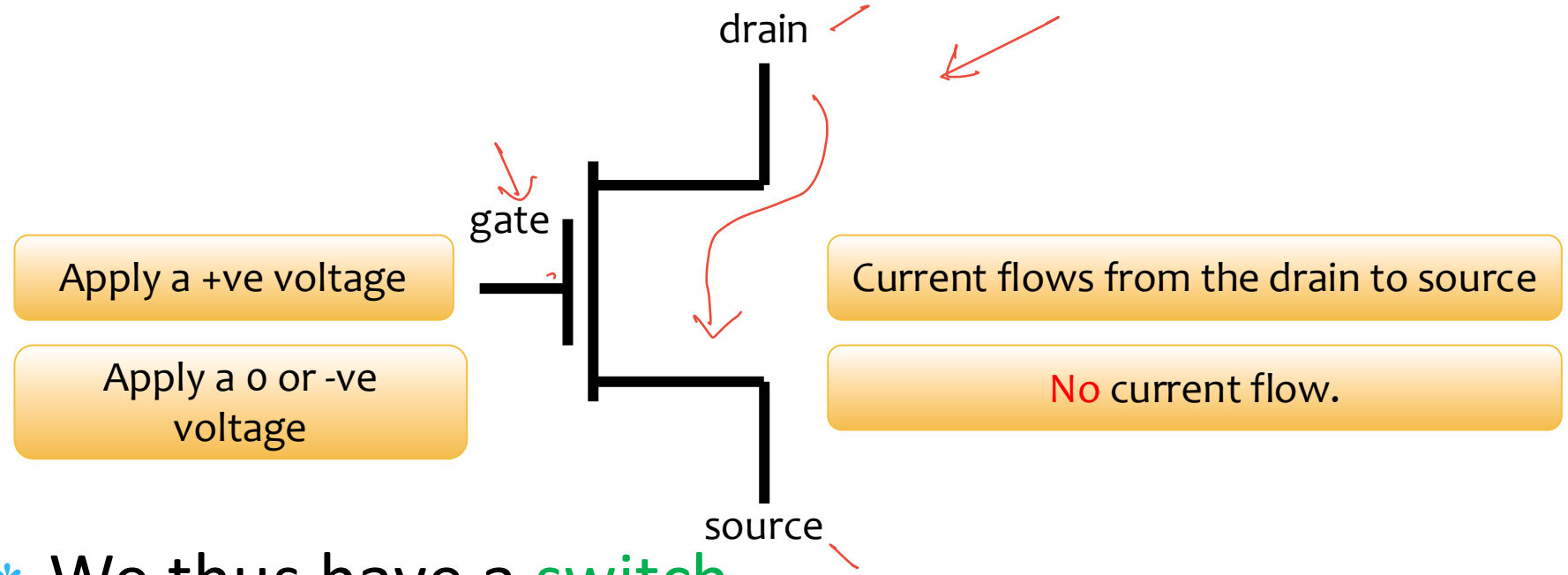
Let us make a transistor.



- NMOS transistor → Put two n-type wells in a p-type substrate
- Now, assume that we apply +ve charge to the gate.
- Channel → This forms because electrons move towards the positive charge. Forms a conductive layer that can conduct current.

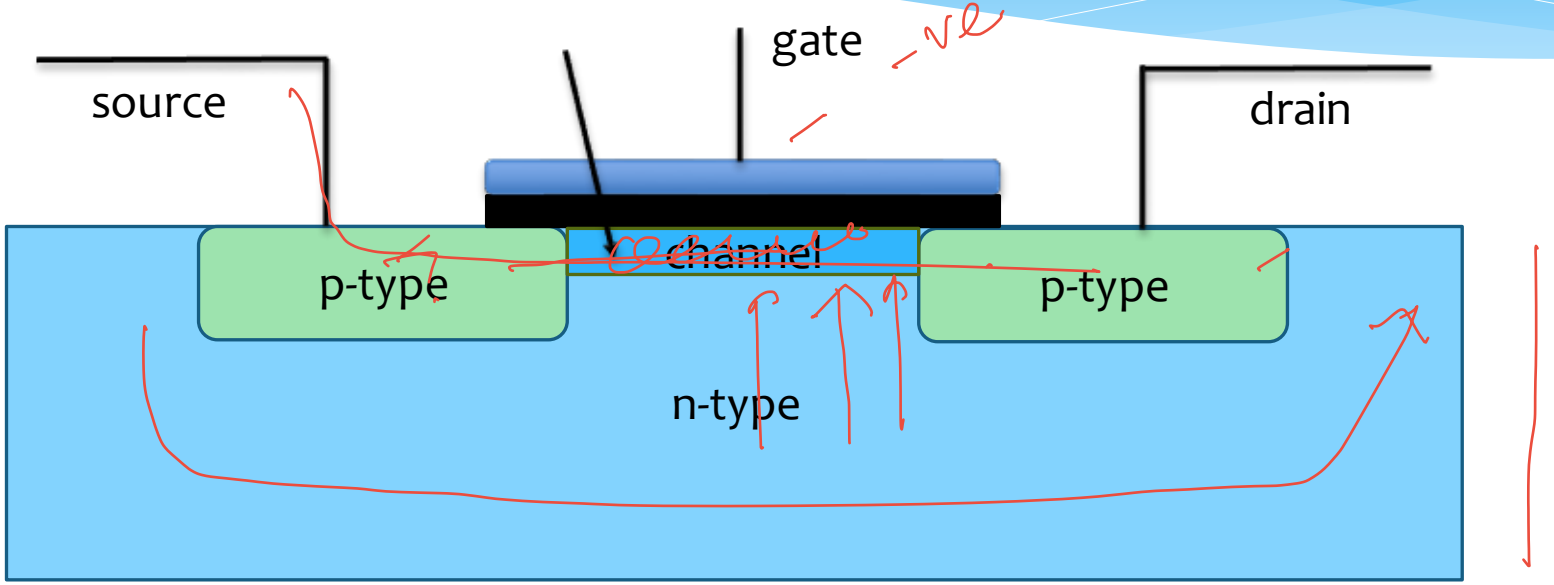
NMOS Transistor

Metal-Oxide-Semiconductor



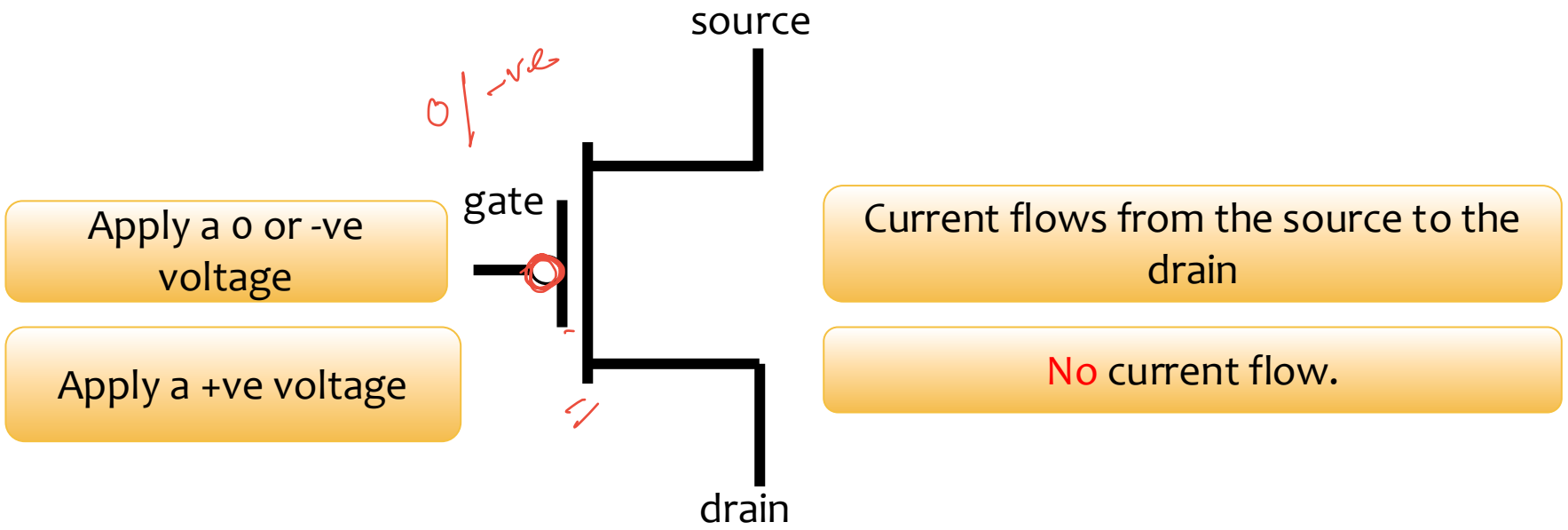
* We thus have a switch
  * Apply a +ve voltage at the gate → make the transistor conduct
  * Apply a –ve or 0 voltage at the gate → transistor is off (no current flow across it)

PMOS Transistor



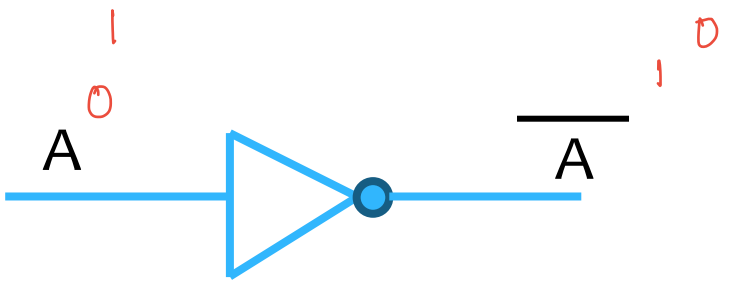
* PMOS transistor → Put two p-type wells in an n-type substrate
* Now, assume we apply 0 or -ve charge to the gate.
* Channel → This forms because holes move towards the gate. This channel can conduct current.

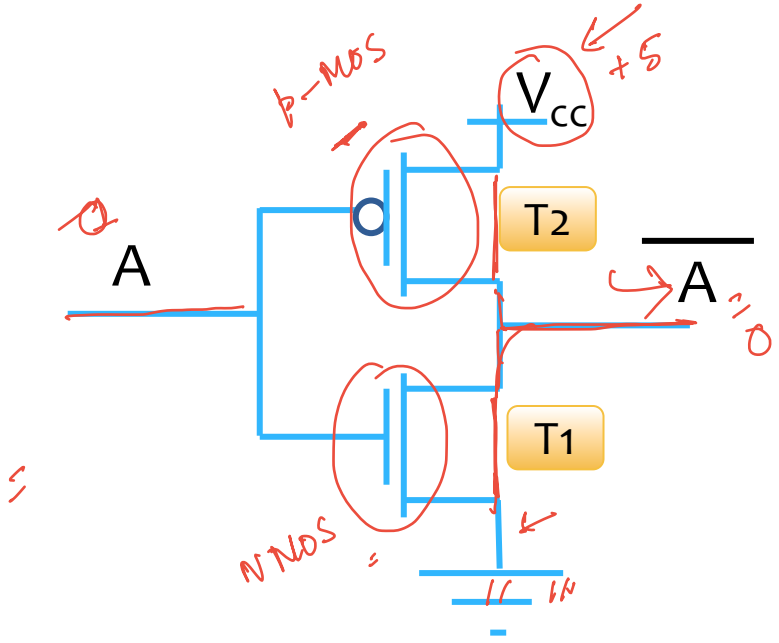
PMOS Transistor



* We thus have a switch
  * Apply a +ve voltage at the gate → transistor is off (no current flow across it)
  * Apply a –ve or 0 voltage at the gate →transistor conducts

Let us make an inverter



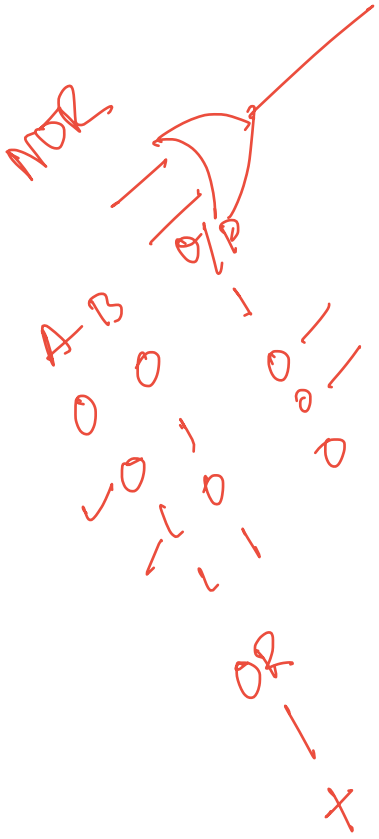


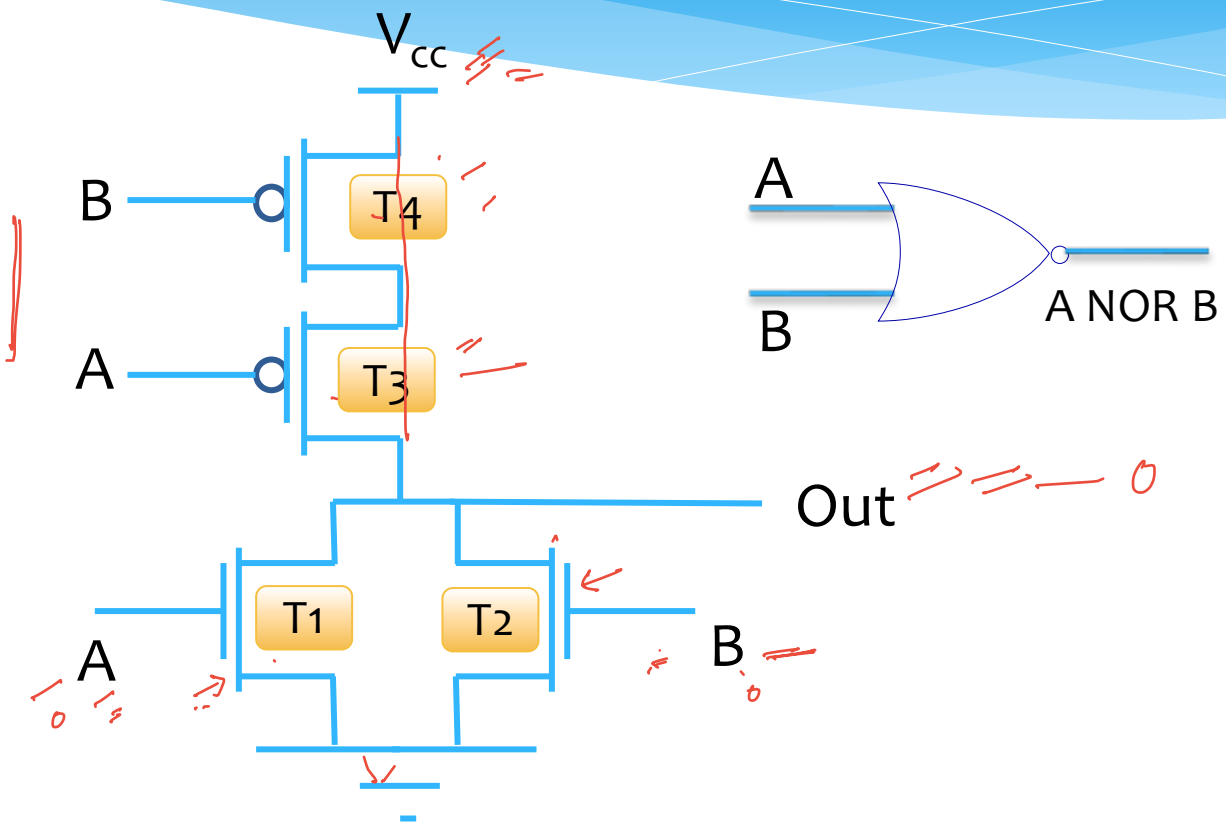
If A = 1 (+ve voltage)
T1 is on, T2 is off
Thus, the output will be connected to the ground, and it will be a logical 0

If A = 0 (0 voltage)
T1 is off, T2 is on
Thus, the output will be connected to the supply (Vcc), and it will be a logical 1

Complementary Metal-Oxide-Semiconductor

NOR Gate



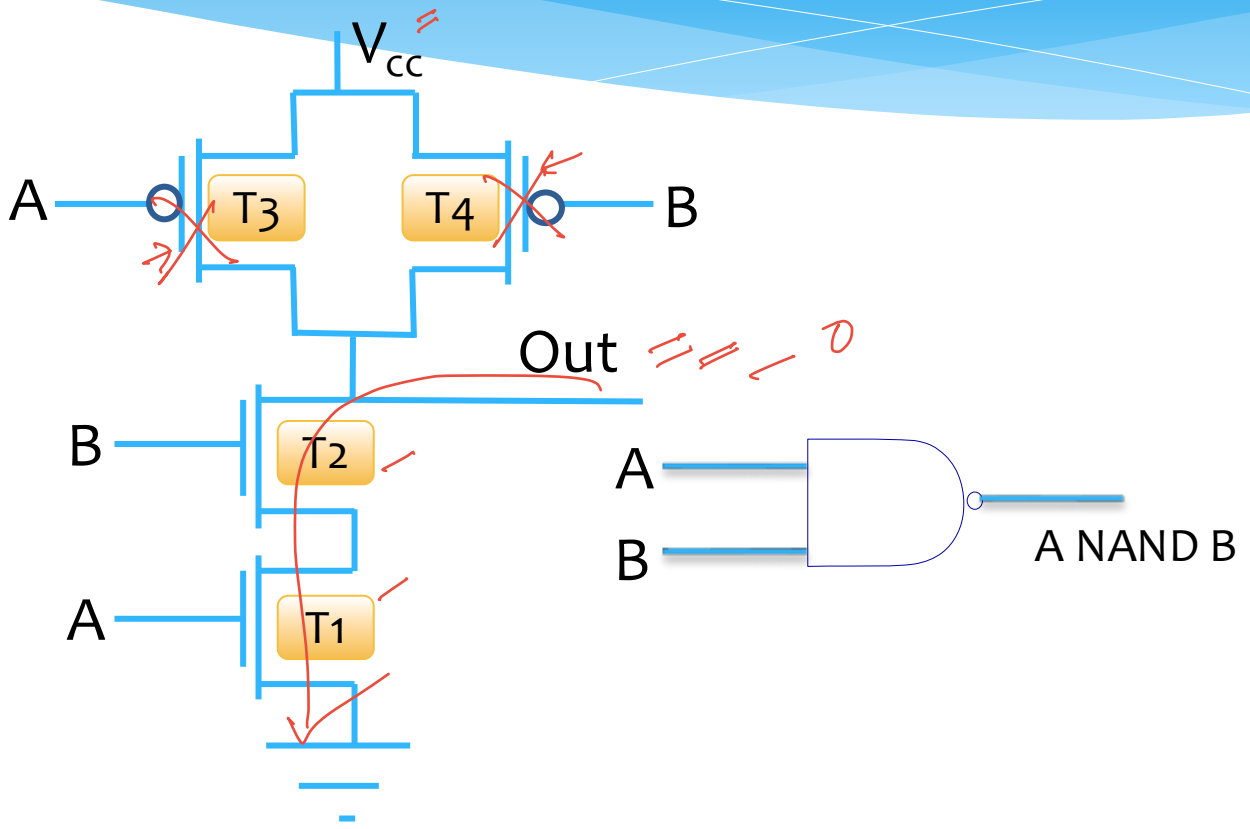


A	B	T1	T2	T3	T4	Out
0	0	off	off	on	on	1
1	0	on	off	off	on	0
0	1	off	on	on	off	0
1	1	on	on	off	off	0

NAND

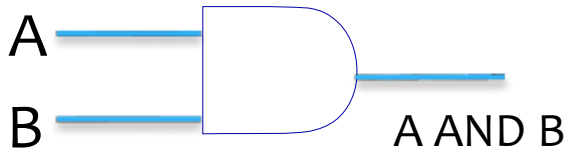
A	B	O/P
0	0	1
0	1	1
1	0	1
1	1	0

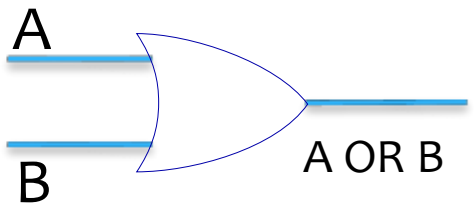
NAND Gate

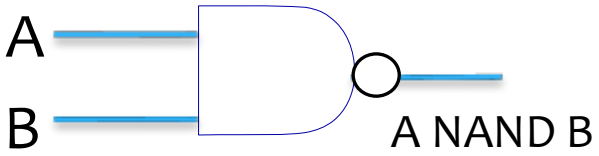


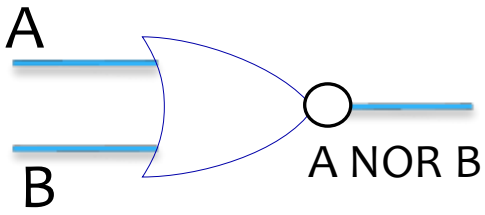
A	B	T1	T2	T3	T4	Out
0	0	off	off	on	on	1
1	0	on	off	off	on	1
0	1	off	on	on	off	1
1	1	on	on	off	off	0

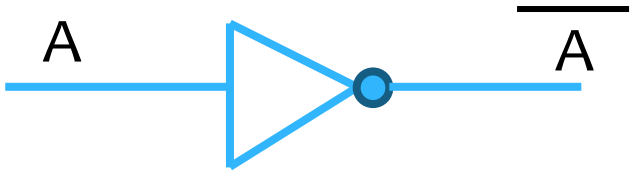
Summary of Logic Gates











Outline

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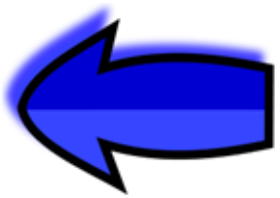
* Combinational Logic 
* Sequential Logic
* SRAM/ DRAM Cells

Mc Graw Hill Education

Multiplexer

Given *n* inputs, choose one based on the select bits.
Example: Given 8 inputs, 3 select bits, choose 1 among them