In-Class Quiz: March 31

Points: 10/10

✓ **Correct** 1/1 Points

1. In the SimpleRisc 5-stage pipeline, which stage is responsible for both breaking the instruction into fields and computing the branch target address (PC + offset)?

- ○ Execute (EX)
- ○ Instruction Fetch (IF)
- ○ Memory Access (MA)
- ◉ Operand Fetch (OF)

✓ **Correct** 1/1 Points

2. In the Instruction Fetch (IF) stage of the SimpleRisc processor, the PC register is negative-edge triggered. If the current instruction is at address A and a branch is not taken, what is the value of the PC after the next negative clock edge?

- ○ A+1
- ○ A+2
- ◉ A+4
- ○ A+8
- ○ None of the above

✓ **Correct** 1/1 Points

3. A processor has a 5-stage pipeline: IF, OF, EX, MA, RW. If a call instruction is executed, in which stage is the return address written to the register file?

- EX
- OF
- MA
- (●) RW
- IF

✓ **Correct** 1/1 Points

4. In the ALU multiplexer logic, if the instruction is add rd, rs1, rs2, what is the value of the isImmediate control signal?

- (●) 0
- 1
- Depends on the value of rs2
- It is not used for add

✓ **Correct** 1/1 Points

5. If the PC is currently at 0x00001000 and a branch instruction b with an offset of 0x0000005 is executed, what is the branchTarget? (Assume the offset is a word offset and the calculation is PC+(offset≪2)

- 0x00001005
- 0x00001010
- (●) 0x00001014

- 0x00001020

✓ **Correct** 1/1 Points

6. Inside the ALU, the isCmp signal is active. What internal hardware component is primarily used, and what is updated as a result?

- Multiplier; updates op1
- Adder; updates the flags register
- Shift unit; updates rd
- Logical unit; updates the PC
- None of the above

✓ **Correct** 1/1 Points

7. In a hardwired control unit, the control signals are functions of the opcode and the state. If the processor is in the "Operand Fetch" stage, and the opcode corresponds to a st (Store) instruction, what must the isSt signal be?

- High Impedance
- Undefined until the EX stage
- 1
- 0

✓ **Correct** 1/1 Points

8. If flags.E=0 and flags.GT=1, and the instruction is bgt (Branch if Greater Than), what is the value of isBranchTaken?

- 0
- 1

- ( ) A+B
- ( ) None of the above

✓ **Correct** 1/1 Points

9. Which of the following instructions would cause the Memory Access (MA) stage to actively interface with the data memory system?

- ( ) add
- ( ) cmp
- (•) st
- ( ) mov

✓ **Correct** 1/1 Points

10. The branchTarget calculation involves shifting an offset and adding it to the PC. If the branch offset is 27 bits, why is it shifted by 2 bits before addition?

- (•) To convert a word-offset into a byte-address.
- ( ) To sign-extend the value to 32 bits.
- ( ) To account for the 2-bit modifier.
- ( ) To multiply the offset by 2.