

In-Class Quiz: March 24

Points: 10/10

✓ **Correct** 1/1 Points

1. How is a logical '1' physically represented within a DRAM cell? 


- By a continuous current flowing through the word line
- By a stored electrical charge across the cell's capacitor
- By connecting the transistor directly to ground
- By the absence of charge in the capacitor

✓ **Correct** 1/1 Points

2. What is the primary function of the Word Line when interacting with a DRAM cell? 

- It permanently stores the data bit.
- It directly amplifies the output voltage.
- It serves as a switch, enabling the access transistor when driven to a logical 1.
- It provides the reference voltage for pre-charging.

✓ **Correct** 1/1 Points

3. Before a read operation begins, the bit line in a DRAM array must be pre-charged. Assuming a logical '1' is represented by 1.0 V, what is the standard pre-charge voltage applied to the bit line? 

- 1.0 V
- 0.0 V
- 2.0 V
- 0.5 V

✓ **Correct** 1/1 Points

4. Because of charge leakage and destructive reads, what critical maintenance protocol must a DRAM system perform?

- Periodically reading each and every cell and writing the same data back
- Discharging the entire array to 0V every millisecond
- Swapping the data between rows to balance wear
- Bypassing the sense amplifiers completely

✓ **Correct** 1/1 Points

5. What immediately happens to the stored charge in a DRAM cell's capacitor as a direct result of performing a read operation?

- The charge doubles due to amplification.
- The charge remains perfectly intact.
- Some charge is lost because it is shared with the long bit line.
- The capacitor becomes permanently polarized.


✓ **Correct** 1/1 Points

6. What is the asymptotic time complexity of an n-bit Ripple Carry Adder?

- $O(\log n)$


- $O(1)$
- $O(n^2)$
- $O(n)$

✓ **Correct** 1/1 Points

7. For an n-bit Carry Select Adder divided into blocks of equal size k, what is the mathematically optimal block size k to minimize the total computation time? 


- $k = n/2$
- $k = \log(n)$
- $k = n^2$
- $k = \sqrt{n}$

✓ **Correct** 1/1 Points

8. If an n-bit Carry Select Adder is divided into individual blocks of size k, how much computational time does Stage II (the sequential selection stage) take to complete? 

- $n \cdot k$ units of time
- n/k units of time
- k^2 units of time
- $n - k$ units of time

✓ **Correct** 1/1 Points

9. If a Half Adder takes time t_1 and a Full Adder takes time t_2 , what is the total computational time required for an n-bit Ripple Carry Adder? 

- $n t_1 + t_2$

- $n t_2$
- $(n - 1) t_1 + t_2$
- $t_1 + (n - 1)t_2$

✓ **Correct** 1/1 Points

10. What specific hardware component is responsible for monitoring this tiny difference in voltage on the bit line during a read operation? 

- The Word Line Decoder
- The Column Multiplexer
- The Sense Amplifier
- The Refresh Driver



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