In-Class Quiz: March 5

Points: 10/10

✓ **Correct** 1/1 Points

1. Why is a standard read operation slow in a large, unoptimized SRAM array?

○ The inverters inside the cell switch very slowly.

○ The word line decoder introduces massive delays.

● Long bit lines introduce high resistance and capacitance.

○ The cross-coupled inverters draw too much current.

✓ **Correct** 1/1 Points

2. When sensing the voltage difference (Δ), what does a positive difference (Δ>0) signify?

$$\Delta = \text{Voltage}(BL) - \text{Voltage}(\overline{BL})$$

○ The cell is empty.

○ A logical 0 is stored.

● A logical 1 is stored.

○ The read operation failed due to noise.

✓ **Correct** 1/1 Points

3. What is the role of the Word Line in an SRAM cell?

○ It transfers the data out of the cell during a read operation.

○ It supplies the constant power (Vcc) to the cell.

○ It continuously refreshes the data in the cell.

● It turns on the access transistors to connect the internal inverters to the bit lines.

✓ **Correct** 1/1 Points

4. What is the primary function of the Column Multiplexer in an SRAM memory array?

○ To boost the voltage of the word line.

● To choose a specific subset of columns to read from or write to.

○ To refresh the data periodically across all columns.

○ To decode the row address.

✓ **Correct** 1/1 Points

5. In a large array of SRAM cells arranged in rows and columns, what component ensures that only one row is accessed at a specific time?

○ Column Multiplexer

○ Sense Amplifier

○ Pre-charge Driver

● Decoder

✓ **Correct** 1/1 Points

6. How is new data written into an SRAM cell?

○ By isolating the bit lines and letting the cross-coupled inverters flip randomly.

● By using strong driver circuits to charge the bit lines to the desired values while the word line is simultaneously enabled.

○ By dropping the word line voltage to 0V and allowing the cell to reset.

○ By applying a higher Vcc directly to the target cell to override its current state.

✓ **Correct** 1/1 Points

7. How is the logical state of the SRAM cell inferred quickly during a pre-charged read?

○ By waiting for one bit line to fully reach 1V and the other 0V.

○ By measuring the current flowing through the word line.

● By monitoring the voltage difference between the two bit lines using Sense Amplifiers.

○ By checking the capacitance of the bit line.

✓ **Correct** 1/1 Points

8. In a 6-Transistor SRAM cell, how many bit lines are required to read from or write to a single cell?

○ 1

● 2

○ 3

○ 4

✓ **Correct** 1/1 Points

9. When utilizing the pre-charging technique, what happens immediately after the word line is enabled?

○ Both bit lines instantly jump to 1V.

○ Both bit lines instantly drop to 0V.

● One bit line voltage starts moving towards 0V, and the other starts moving towards 1V.

○ The cell's internal state is wiped out.

✓ **Correct** 1/1 Points

10. What is the fundamental storage component within a standard SRAM cell?

○ A cross-coupled pair of NAND gates

● A cross-coupled pair of inverters

○ A single capacitor and a transistor

○ A combination of multiplexers and decoders