

In-Class Quiz: Feb 26

Points: 10/10

✓ **Correct** 1/1 Points

1. Why is JK flip-flop considered more versatile than D flip-flop? (FF with NAND)



- It uses fewer gates
- It can implement SR, D, and T behaviors
- It is asynchronous
- It needs no clock

✓ **Correct** 1/1 Points

2. How many NAND Gates are present in a Master Slave D Flip Flop? 

- 4
- 8
- 12
- 10


✓ **Correct** 1/1 Points

3. The fundamental advantage of D flip-flop over SR flip-flop is:




- Faster operation
- No race condition
- Elimination of invalid state
- Lower power consumption

✓ **Correct** 1/1 Points

4. Why is a clock added to a basic NAND SR latch? 

- To eliminate propagation delay
- To prevent invalid condition
- To control when input affects output
- To increase fan-out

✓ **Correct** 1/1 Points

5. In a NAND-based clocked SR latch, when the clock is LOW, the latch: 

- Toggles
- Becomes transparent
- Holds its previous state
- Goes to invalid state

✓ **Correct** 1/1 Points

6. The slave latch in a master–slave D flip-flop is active when: 

- clock = 1

- clock = 0
- Both clock = 0 and clock = 1
- None

✓ **Correct** 1/1 Points

7. Which of the following is used for storing one bit: 

- Encoder
- Decoder
- D-Flip Flop
- Mux


✓ **Correct** 1/1 Points

8. When $J = 1$ and $K = 0$ in Master–Slave JK FF (NAND Gate), the output:



- Resets
- Sets
- Toggles
- Holds

✓ **Correct** 1/1 Points

9. The major drawback of a clocked NAND latch is: 

- High power
- Edge-triggered behavior

Level-sensitive behavior

Cannot store data

✓ **Correct** 1/1 Points

10. Why is the Master–Slave D flip-flop (With NAND Gate) edge-triggered?



Because NAND gates are fast

Because data propagates only during clock transition

Because clock frequency is high

Because feedback is removed



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