In-Class Quiz: Feb 24

Points: 10/10

✓ **Correct** 1/1 Points

1. In a standard NAND SR Latch configuration, what happens to the stored data when the inputs are dropped to S=0 and R=0?

- ○ The latch resets
- ○ The latch sets
- ◉ The latch maintains its old values
- ○ The latch enters a forbidden state

✓ **Correct** 1/1 Points

2. If a demultiplexer has 5 select bits, what is the maximum number of output lines it can support?

- ○ 5
- ○ 10
- ○ 25
- ◉ 32

✓ **Correct** 1/1 Points

3. What is the minimum number of 2:1 MUXs required to design a 4:1 MUX?

- 2
- 3
- 4
- 5

✓ **Correct** 1/1 Points

4. In the logical construction of an 8-to-3 encoder, multiple input lines are fed into OR gates to generate the binary output. Which specific input bits determine the least significant bit (Bit0) of the output?

- b4,b5,b6,b7
- b2,b3,b6,b7
- b1,b3,b5,b7
- b0,b2,b4,b6

✓ **Correct** 1/1 Points

5. An 8-to-3 encoder's output is directly wired to the input of a 3-to-8 decoder. If the 4th input line (b4) of the encoder is activated , which output line of the decoder will subsequently be set to 1?

- Line 2
- Line 3
- Line 4
- Line 8

✓ **Correct** 1/1 Points

6. A processor needs to read data from one of 250 distinct memory banks. It uses a

multiplexer to route the data from the chosen memory bank to the CPU. What is the minimum number of select lines this multiplexer must have to handle all 250 inputs?

- 7
- 8
- 9
- 250

✓ **Correct** 1/1 Points

7. A Clocked NAND SR Latch requires a clock signal to update its state. If the clock signal is currently 0, how does the latch respond to changes on the S and R input lines?

- It behaves exactly like a classic SR latch.
- It forces the outputs to 0.
- It enters a high-impedance state.
- It ignores the inputs and maintains its old values.

✓ **Correct** 1/1 Points

8. An encoder takes n inputs (assuming only one is active) and finds its binary ID. If the 5th input out of 8 inputs is the only one set to 1, what will the 3-bit binary output (Bit2, Bit1, Bit0) be?

- 100
- 101
- 110
- 111

✓ **Correct** 1/1 Points

9. When evaluating the logical states of a NAND SR Latch, which input combination is strictly avoided because it leads to an undefined state where the outputs do not properly complement each other?

- ○ S=0, R=0
- ○ S=0, R=1
- ○ S=1, R=0
- ◉ S=1, R=1

✓ **Correct** 1/1 Points

10. In a Clocked NAND SR Latch, the clock transitions to 1. While the clock is 1, the inputs are set to S=0 and R=1. What is the resulting state of Q?

- ◉ Q=0
- ○ Q=1
- ○ Q toggles based on the clock frequency.
- ○ Q maintains its previous state.