


# In-Class Quiz: April 2

Points: 15/15

✓ **Correct** 1/1 Points

1. A bgt instruction is fetched from memory address 0x08000020. If the branch condition is met, the next instruction fetched is from 0x0800004C. What is the exact 27-bit binary offset embedded within the instruction encoding? 


0...01011

0...10110

0...01100

0...2A000

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2. An add instruction utilizes an 18-bit immediate value of 0x2F1A4. During the Operand Fetch (OF) stage, this immediate is sign-extended to 32 bits to produce immx. What is the 32-bit hexadecimal value of immx supplied to the ALU? 

0x0002F1A4

0xFFFFF1A4

0x8002F1A4

0xFFFFF1A40

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3. Assume register r4 contains the value 0x00004000. The instruction `ld r3, -8[r4]` is currently executing. During the Memory Access (MA) stage, what exact 32-bit value is placed into the Memory Address Register (MAR)?

0x00003FF8

0x00004008

0xFFFFFFFF8

0x00004000

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4. The processor fetches a 32-bit instruction with the hexadecimal encoding 0x78000000. Based strictly on decoding the top 5 bits, what will be the boolean values of the `isSt`, `isLd`, and `isWb` control signals in the OF stage?

`isSt=0, isLd=1, isWb=1`

`isSt=1, isLd=0, isWb=1`

`isSt=1, isLd=0, isWb=0`

`isSt=0, isLd=0, isWb=0`

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5. A call instruction is located at address 0x1000A004. During the RW stage of this instruction, a multiplexer routes a specific value to the write data port of the register file. What is the precise numerical value written, and to which register address?


0x1000A004 to rd

0x1000A008 to ra(15)

0x1000A008 to rd

0x1000A004 to ra(15)


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6. Consider the hardwired control logic for the isUbranch signal given below. Which of the following opcodes will NOT evaluate to 1 for this equation? 

$$isUbranch = op5 \cdot \overline{op4} \cdot (\overline{op3} \cdot op2 + op3 \cdot \overline{op2} \cdot \overline{op1})$$


- 10010
- 10011
- 10100
- 10000

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7. According to the provided control unit boolean logic, the isCall signal is defined simply as:  $isCall = op5$ . Given that the opcode for beq is 10000, what unintended hardware conflict would this simplified boolean equation cause during the execution of a beq instruction? 

- It would force the ALU to perform an addition instead of a comparison.
- It would overwrite the return address register ra(15) with PC+4 in the RW stage.
- It would cause the IF multiplexer to unconditionally take the branch.
- It would stall the pipeline in the OF stage.

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8. Evaluate the isWb boolean expression for a nop instruction (opcode 01101), as given below. What does this expression mathematically reduce to for this specific instruction? 

$$isWb = \sim (op5 + \overline{op5} \cdot op3 \cdot op1 \cdot (op4 + \overline{op2})) + op5 \cdot op4 \cdot op3 \cdot op2 \cdot op1$$

- $1 + 0 = 1$
- $0 + 1 = 1$

$\sim (1) + 0 = 0$

$\sim (0) + 0 = 1$

✓ **Correct** 1/1 Points

9. The isRet signal serves as the selector for two distinct multiplexers across different pipeline stages. Which two values are ultimately brought face-to-face at the final IF stage PC multiplexer when isRet = 1?

branchTarget and PC+4

The contents of ra(15) and PC+4

immx and PC+4

aluResult and branchTarget

✓ **Correct** 1/1 Points

10. If flags.E = 1 and flags.GT = 0, and the fetched instruction is bgt 0x00000008, what arithmetic calculation ultimately determines the updated Program Counter value in the IF stage?

PC + 0x00000008

PC + 4

PC + 0x00000020

ra(15)


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11. To optimize power, the ALU utilizes transmission gates at the inputs of its functional units. If the processor decodes a cmp r1, r2 instruction, what are the logic states of the control signal S for the transmission gates feeding the Adder and the Logical Unit, respectively?

Adder S=1, Logical Unit S=1


- Adder S=0, Logical Unit S=1
- Adder S=1, Logical Unit S=0
- Adder S=0, Logical Unit S=0

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12. An instruction requires calculating an extended immediate value (immx) while simultaneously decoding the opcode to generate the isWb signal. In which specific pipeline stage boundary do both of these distinct hardware operations physically reside? 

- Instruction Fetch (IF)
- Operand Fetch (OF)
- Execute (EX)
- Between EX and Memory Access (MA)

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13. During the OF stage, the register file receives inputs to its Read Port 2. If the isSt (Store) signal is active (1), which bits of the 32-bit instruction format directly dictate the address fed into Read Port 2? 

- Bits 15:18
- Bits 19:22
- Bits 23:26
- Bits 28:32


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14. The ret instruction uses the I bit (bit 27) in its encoding. Architecturally, why is the specific value (0 or 1) of the I bit completely irrelevant to the correct execution of the ret instruction

in the EX stage? 

- The isRet multiplexer overrides the ALU output, bypassing the immx vs op2 selection entirely.
- The I bit is physically disconnected from the ALU during branch instructions.
- The ALU forces a logic 0 on all inputs when isRet = 1.
- ret does not use the EX stage.

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15. Trace the hardware path of branchTarget. Before it reaches the EX stage multiplexer, it is calculated in the OF stage using an Adder. What are the two specific 32-bit inputs to this dedicated OF stage Adder? 

- op1 and immx
- PC and immx
- PC and Offset (shifted 2 bits and sign-extended)
- PC+4 and Offset



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